

Control Strategies for Capacitor Voltage Balancing in Modular Multilevel Converters

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Abstract- Different schemes of modified conventional sorting algorithms with low complexity are proposed in order to balance the voltages of submodule (SM) capacitors for the modular multilevel converter (MMC). Two different procedures are investigated in this study. The main idea is to achieve voltage balance within the MMC arms with fewer current sensors. The two different methods are examined under different operating conditions; for instance, with a sudden change in the DC-source or when different load values are applied. The advantage of such sensor-less control methods is to simplify hardware communications in general. Moreover, the reliability of the MMC is also improved. Simulation analyses of a single-phase four-level MMC are conducted to show the effectiveness of the proposed methods.

Keywords—; *Modular Multilevel Converter; PWM; Voltage balancing control; sorting algorithm .*

I. INTRODUCTION

The modular multilevel converter (MMC) has shown highly attractive features since being introduced in 2003 by Lesnjar and Marquardt [1]. The MMC consists of a series of cascaded sub-modules (SMs) with a couple of arm inductors for each phase. This serial structure gives the converter a number of superior features, when compared with conventional converters, such as: flexibility in the structure, low harmonic distortion achieved due to the high voltage levels of the converter, and low switching losses. Moreover, the arm inductors within each phase play a key role when faults occur [2-4]. Furthermore, these inductors can minimize the ripples across the SM capacitor.

Due to its aforementioned characteristics, the MMC can be considered as a very promising candidate for some medium- and high-power applications. This includes flexible AC transmission systems (FACTS), high-voltage direct current (HVDC) systems, dynamic braking choppers, variable speed drives and battery storage systems [5-7]. The MMC can also be used for large-scale multistring photovoltaic energy conversion systems [8]. In this case, the input of each module of the MMC is a dc-dc converter controlled by a maximum power point tracking algorithm similar to those presented in [9-11]. Therefore, the MMC will probably be used in many future power systems applications.

On the other hand, various challenges associated with this topology are still under investigation, such as capacitor imbalance issue, circulating current issues, and the high number of the sensors required [12]. However, there is also substantial research going in this area to overcome these challenges. For example, the capacitor imbalance issue has been investigated in several studies. The phase shifted-pulse width modulation (PS-PWM) technique has been applied to the converter in a method based upon two main steps: averaging and balancing control [13]. A selective harmonic elimination-PWM (SHE-PWM) scheme has also been applied to the converter with the aim of achieving the lowest harmonic and switching frequency losses [14]. Another well-known proposal is called the sorting algorithm method, where the idea is to select the most suitable SM which has to be charged or discharged with regardless to the switching frequency value [15, 16]. Nevertheless, in all of the aforementioned strategies, the monitoring of the SM voltage capacitors and the phase current (i.e. the upper and lower arm current) is essential. Despite this, some studies have achieved capacitor balancing without using voltage transducers, for example by using an observer based on the Kalman filter algorithm [12], an adaptive observer based on the Lyapunov function [17], and a prediction-correction method [18]. However, voltage balancing has rarely achieved with fewer current sensors.

In this paper, voltage balancing control methods are proposed for the MMC. These methods are based on modification of the conventional sorting algorithm scheme. Two different procedures are investigated. The idea is to demonstrate the ability to balance the SM voltage capacitors with fewer current sensors by modifying the conventional sorting algorithm used in previous studies [15, 16]. Despite the use of open loop control methods such as the ones introduced in a recent study [19], not many studies deal with voltage balancing issues using fewer current sensors. For example in two recent studies [20, 21] different methods have been introduced showing both simulation and practical results. High frequency current components have been controlled for the SM capacitors under different operating conditions [20]. Alternatively, the switching frequency of the semiconductor switch may be controlled and minimized [21]. In both methods, only the PS-PWM technique can be used. However, the methods introduced in the present research can use different PWM techniques such as, PS-PWM and phase disposition-

PWM (PD-PWM)). Moreover, the effectiveness of the proposed methods has been successfully proven for a four-level MMC with operating conditions which include: abrupt variations in the DC-source and when applying different load to the system. Therefore, the proposed methods can easily minimize the complexity of the converter as well as improving its reliability.

II. OPERATION AND STRUCTURE OF THE MMC

For simplicity, only a single phase is considered in this research. Fig 1 shows the structure of a single-phase MMC. This phase comprises of two arms (upper arm and lower arm), and along with each arm there is a conductor (arm conductor (L_s)). The value of the two conductors should be equalized. The summation of the upper and lower arm components is called a single leg. The converter contains a series connection of half-bridge SMs ($SM_1, SM_2, \dots, SM_{2n}$). The resistance of these SMs is very small; therefore it has been neglected in Fig 1. Fig 2 illustrates the configuration of the half-bridge SM. Each SM has two semiconductor IGBT or MOSFET switches and a capacitor. The two switches (S_1 and S_2) in Fig 2 are controlled in a complementary method. Table 1 depicts the required procedure for S_1 and S_2 from the controller. Once the S_1 is on, the output voltage SM (V_{SM}) will be equal to the voltage across the capacitor (V_c). Whereas, when S_1 is off, the voltage value of V_{SM} is zero. Consequently, V_c will be bypassed in the circuit.

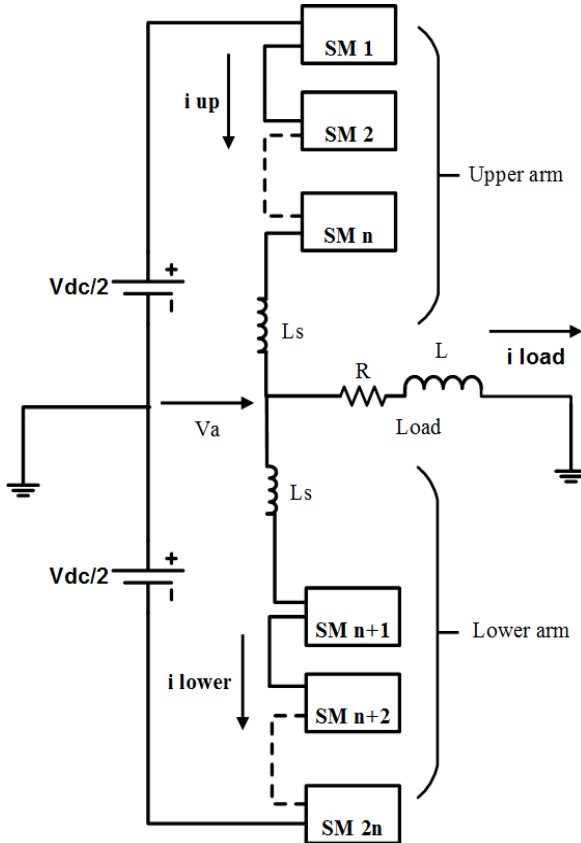


Fig. 1. Single-phase MMC configuration.

Table. 1. Switching states of the SM.

State of the SM	S_1	S_2	V_{SM}
On	1	0	V_c
Bypassed	0	1	0

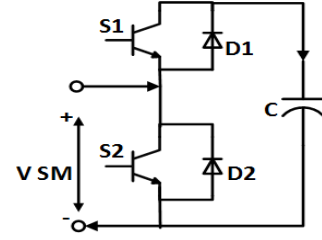


Fig. 2. Configuration of SM.

The upper and lower arm currents are described as follows [22]:

$$i_{up} = i_{cir} + (i_{Load}) / 2 \quad (1)$$

$$i_{lower} = i_{cir} - (i_{Load}) / 2 \quad (2)$$

where i_{cir} , i_{up} , i_{lower} , and i_{Load} are circulating current, upper arm current, lower arm current and load current respectively. The output voltage (V_a) of the converter can be expressed as:

$$V_a = L_{Load} ((di_{Load}) / dt) + R_{Load} i_{Load} \quad (3)$$

III. PROPOSED VOLTAGE BALNCING CONTROL METHODS.

In the conventional sorting algorithm as presented in recent researches [15, 16], monitoring the upper and lower arm currents of each phase is necessary in order to achieve a good voltage balance in the converter. In this research, however, achieving voltage balancing is guaranteed by two different approaches: in the first there is one current sensor for each leg and the second method involves no current sensor at all. Note that the steps of the conventional method comprises of a reference signal, carrier signals, the number of SMs involved as well as part of the conventional method block as illustrated in Fig 3. The next section describes the proposed methods in detail.

A. Load Current Monitoring Method

Compared with the conventional sorting algorithm method, only one sensor per leg is required to monitor the load current. The charging and discharging of the SM capacitors relies on the direction of the load current. If the load current is positive, the upper targeted SM capacitors which have the lowest value will be charged. If the load current is negative, on the other hand, the targeted SM capacitors (the capacitors with the highest values) will be discharged. In both cases S_1 must be on and S_2 must be off. Identifying the required SM capacitor is based on the sorting mechanism as shown in Fig 3.

For the lower arm, the same principle applies; however an inverted load current ($i_{inv-Load}$) is inserted into the algorithm which satisfies the following formula:

$$i_{Load} + i_{inv-Load} = 0 \quad (4)$$

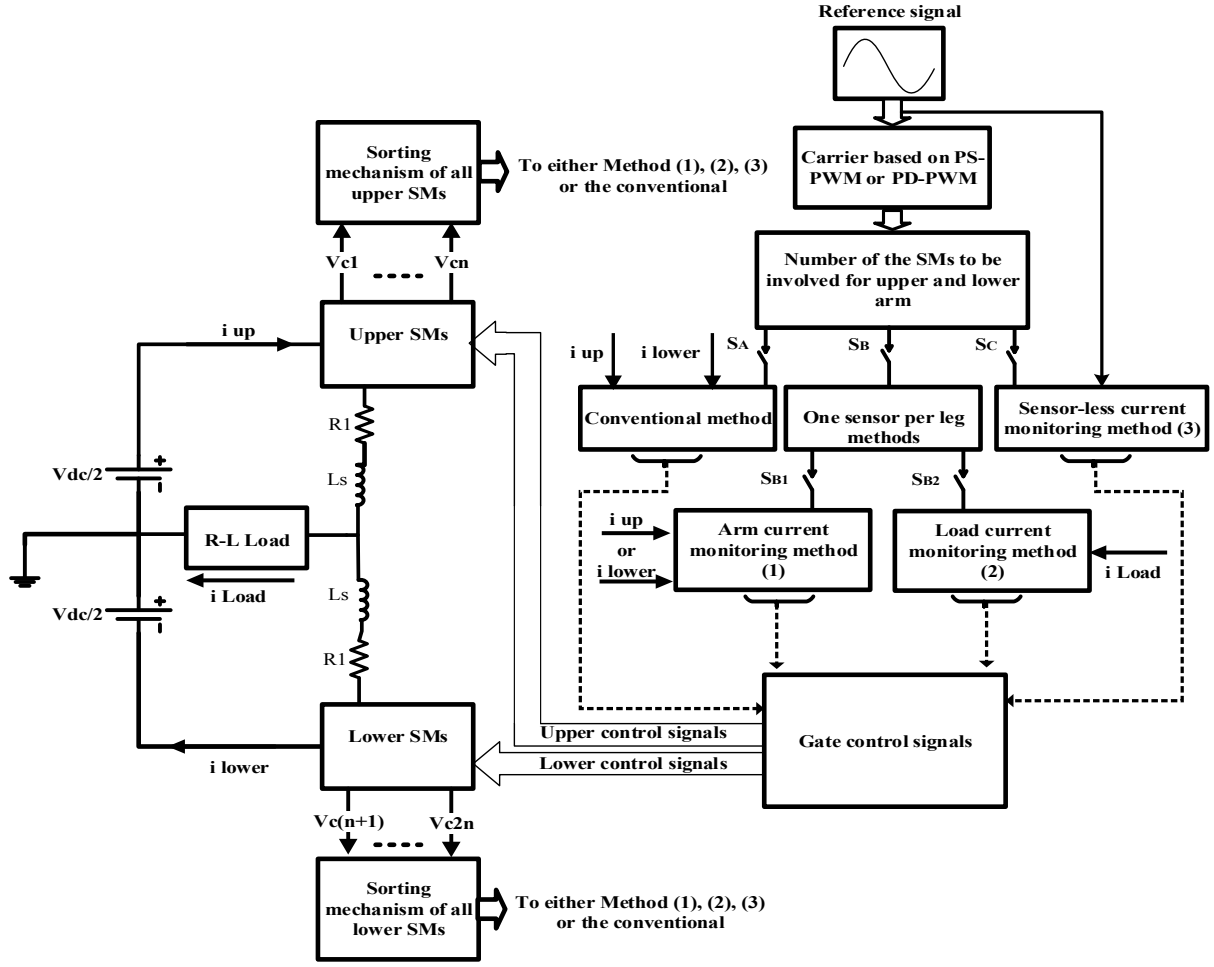


Fig 3. General block diagram of the proposed methods, indicating contrast with the conventional sorting algorithm.

In Fig 3, switches S_A , S_B , and S_C are only used to distinguish between the methods. For instance, when applying the load current monitoring method, S_B should be on whilst S_A and S_C must be off.

B. Sensor-never Current Monitoring Method

Similar to the conventional method, a sine wave reference signal ($\sin 2\pi ft$), carrier signals and the number of SMs to be involved are applied. However, the charging and discharging of the converter capacitors are based on the $\sin 2\pi ft$ direction. For the upper arm SMs, as in the load current monitoring method, the lowest capacitors will be charged and the highest capacitors will be discharged, but the reference signal ($\sin 2\pi ft$) will make the decision concerning the status of the (charging or discharging) rather than the load current direction. For controlling the lower arm capacitors, the reference signal is shifted by $\pm \pi$ to the lower half of the converter.

In the case of HVDC systems or any closed loop application where the MMC is connected to the grid, the duty cycle of the closed loop controller can be used for the algorithm. In other words, the decision about which capacitor is being charged or discharged will depend on the direction of the controlled duty cycle.

To fully validate these methods, the next section discusses the effect of changes in operating conditions.

IV. SIMULATION RESULTS

Fig 4-6 illustrate simulated waveforms from Fig 3 and Table 2 summarized the system parameters. The results in these figures were achieved using the MATLAB software package.

Fig 4 shows the performance of the single-phase four-level MMC under normal operation conditions. The output load voltages and voltages at C_1 of the three methods (conventional method, load current monitoring method and sensor-never monitoring method) are depicted in the same Fig 4 (a-f). The reference voltage signals for all three methods were evaluated at 50 Hz.

Fig 5 investigates the performance of the proposed methods compared to the conventional method where a sudden change in the DC-source is applied at 0.8s. The DC-source is increased by 50% from 480v to 720v at 0.8s. Fig 5 (a-c) shows the voltages at C_1 of the conventional sorting algorithm method, load current monitoring method and sensor-never current monitoring method respectively. In these selected results the

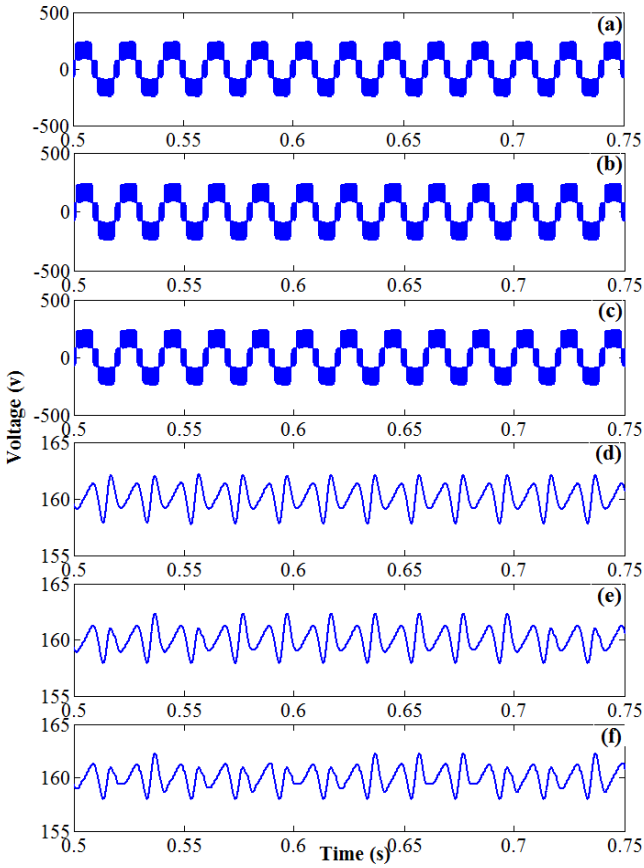


Fig 4. Output load voltages and voltages at C_1 of the three methods: (a) and (d) conventional sorting algorithm method; (b) and (e) load current monitoring method; (c) and (f) sensor-less current monitoring method.

arm capacitors are assumed to be pre-charged (i.e. the initial value is V_{dc}/n), where n is the summation of all SMs within the upper or lower arm. For a four-level MMC, n is 3.

Table 2. Simulation parameters for single phase four-level MMC.

Parameters	Value
Modulation index (mi)	0.9
DC-link voltage (V_{dc})	(480 & 720) V
Number of SMs (n)	3
Switching frequency	2.5 k Hz
Load resistor (R)	33 Ω
Inductive load (L)	(1.2, 2.4 & 24) mH
SM capacitor	1.5 mF
Arm inductance (L_s)	1 mH

The inductive load is 1.2 mH. It can be noted that the settling times of the proposed methods shown in Fig 5 (b) and (c) are less than that for the conventional sorting algorithm method (Fig 5 (a)), which is in turn reflected in the output load voltage waveforms as shown in Fig 6 (a), (b), and (c) respectively.

To further validate the proposed methods, the load in Fig 3 is applied with three different phase shifts between the inductor

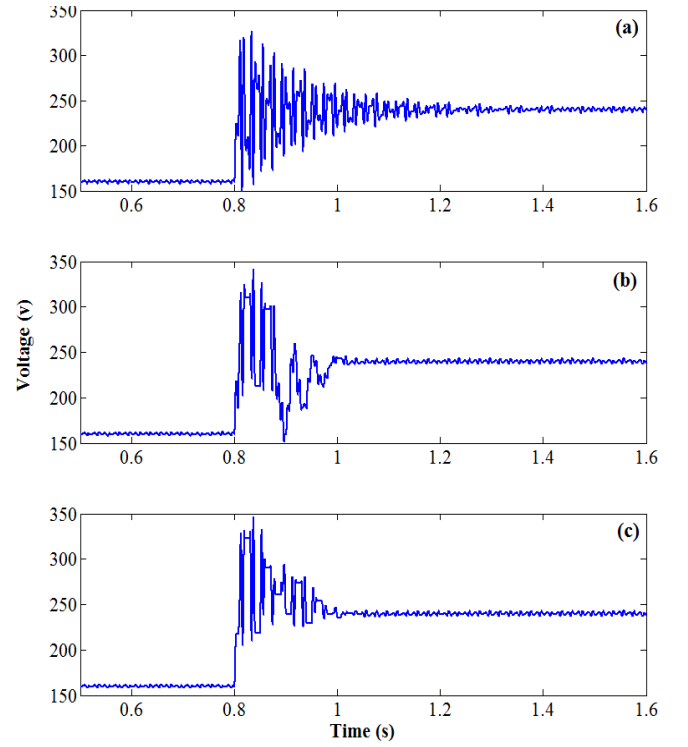


Fig 5. Voltage waveform across SM_1 capacitor for the three methods: (a) conventional sorting algorithm method; (b) load current monitoring method; (c) sensor-less current monitoring method.

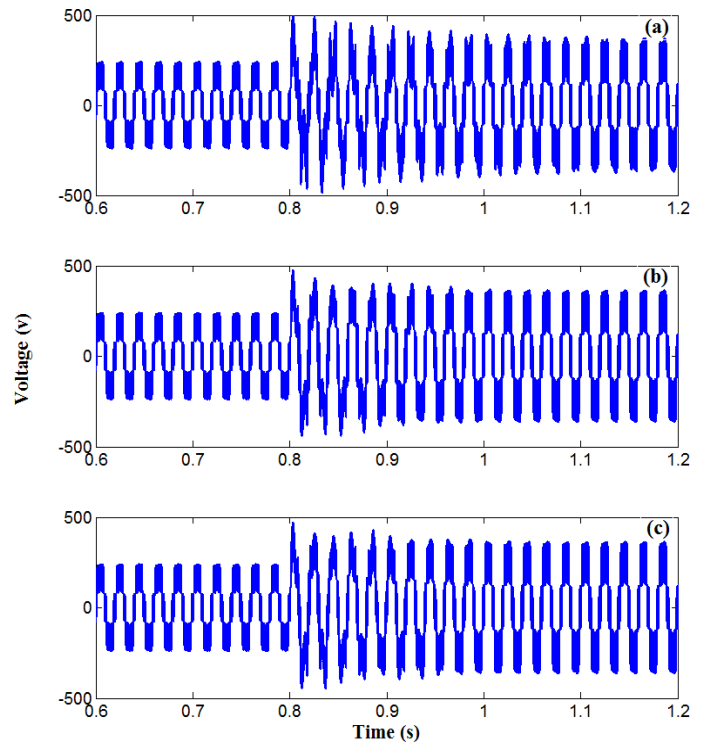


Fig 6. Output load voltage waveforms for the three methods: (a) conventional sorting algorithm method; (b) load current monitoring method; (c) sensor-less current monitoring method.

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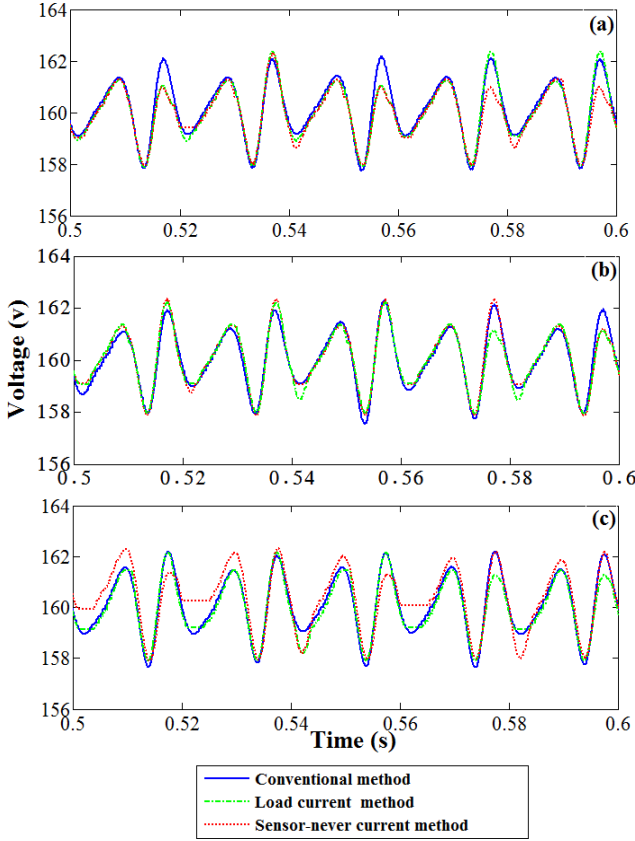


Fig 7. V_{c1} with three different values of inductive load for the three methods; (a) 1.2 mH applied to the three methods. (b) 2.4 mH applied to the three methods. (c) 24 mH applied to the three methods.

(L) and resistor (R) (i.e. output load voltage and current). The three different values of the load inductors (1.2, 2.4 and 12 mH) are shown in Fig 7 (a), (b) and (c) respectively.

Comparing the present simulation results with those of the conventional method, the proposed methods show some superiority in the simulation environment under different operating conditions. However, care has to be taken when choosing the SM capacitor value, because some small values will cause offsets in both proposed methods. This is probably due to resonance issues; therefore further practical work will be carried out to validate the methods.

V. CONCLUSION

In this paper, voltage balancing control methods are proposed for the MMC. Two methods are investigated. The first involves only one current sensor, while the second method achieves voltage balancing without any current sensors; both methods show some superiority in terms of settling time. Moreover, there are no big differences among the methods when the phase shifts between the output voltage and current varied. Simulation studies with MATLAB software have verified the proposed methods for a four-level MMC. Therefore, the idea can minimize complexity as well as improve the reliability of the MMC.

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